EUVL Mask Substrate Specifications (wafer type)

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July 1, 1999

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EUVL mask substrate specifications (wafer type)

(Rev. 0.2, September 99)

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I.   Abstract

The Extreme Ultraviolet Lithography (EUVL) program currently is constructing an alpha-class exposure tool known as the Engineering Test Stand (ETS) that will employ 200mm wafer format masks. This document lists and explains the current specifications for the EUVL mask substrates suitable for use on the ETS.

• The shape and size of the mask are the same as those of a standard 200mm Si wafer.

• The flatness requirements are driven by the potential image placement distortion caused by the non-telecentric illumination of EUVL.

• The defect requirements are driven by the printable-defect size and desired yield for mask blank fabrication.

• Surface roughness can cause both a loss of light throughput and image speckle.

• The EUVL mask substrate must be made of low-thermal-expansion material because 40% of the light is absorbed by the multilayers and causes some uncorrectable thermal distortion during printing.

II.   Introduction

EUVL is a leading candidate to be the Next Generation Lithography (NGL) currently proposed to be inserted at the 70nm node.   One of the key differences between EUVL and conventional optical lithography is that EUVL employs light that is 13.4nm in wavelength.   Since the EUVL mask is reflective and coated with Mo/Si multilayers, its requirements and properties are significantly different from today's photomask. Mask substrates with the shape of 200mm silicon wafer will be required through at least Y2001 for use on the ETS. The purpose of this report is to list the current specifications for the EUVL mask substrates and to explain in detail the reasoning behind each specification. It is important to note that a 152mm square and 6.35mm-thick format standard is under discussion for beta- and production-class EUVL tools.

It is imortant to note that these specifications are subject to modifications as our needs are constantly evolving.   Please e-mail for any updates, questions, or comments.
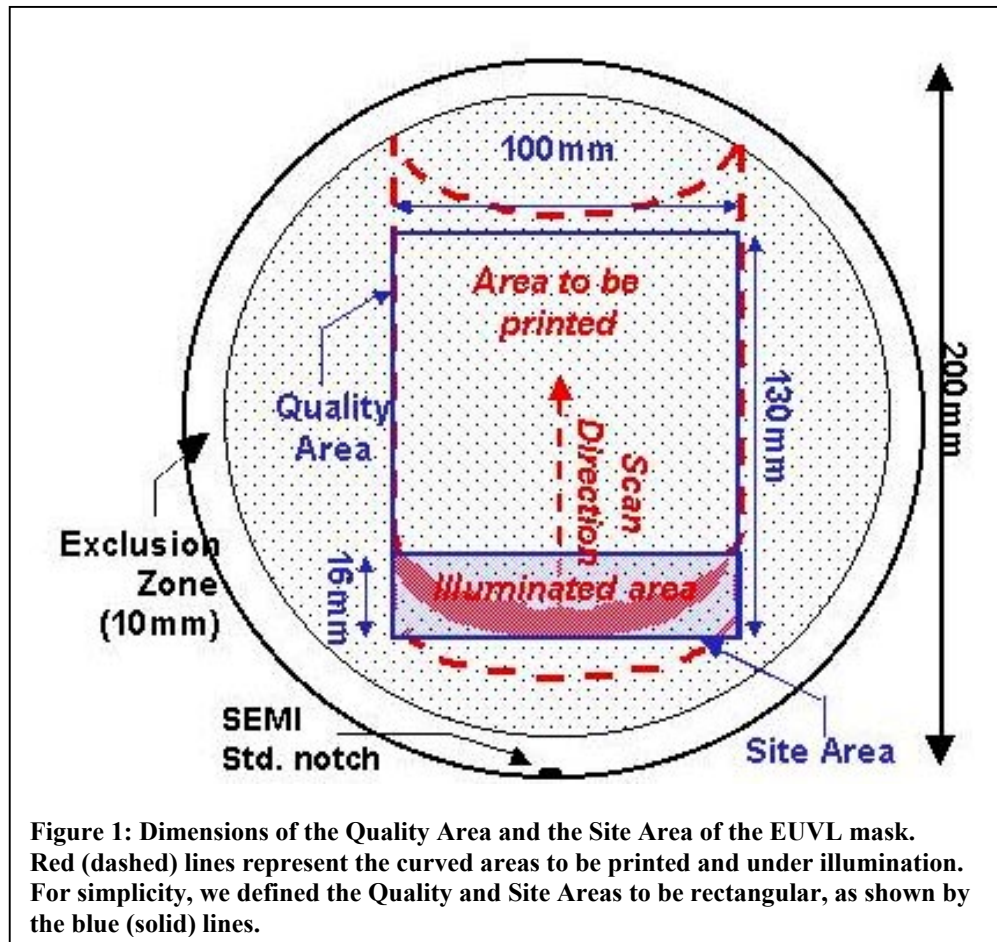
III. EUVL mask substrate specifications Rev. 0.1 (September 1999)

Item no.	Total Wafer Characteristics	Units	Metric Criteria
	Shape Specifications		
1.	Diameter	mm	200 ± 0.2
2.	Mean thickness	μm	725 ± 15
3.	Global Total Indicator Reading (GTIR)	μm	≤ 2.0 (within radius ≤90 mm)
4.	TTV (Total Thickness Variation)	μm	≤ 1.0 (within radius ≤90mm)
5.	SFSR (Quality Area = 130mm x 110mm Site Area = 16mm x 110 mm)	μm	≤ 0.2 (in any 16mm x 110mm Site Area inside Quality Area)
6.	**Frontside LPD (light-point defects) density**		
6a.	Size ≥ 0.08 μm	LPD/wafer	≤ 3
6b.	Size ≥0.13 μm	LPD/wafer	≤ 1
6c.	Size ≥ 20 μm	LPD/wafer	None
7.	**Surface Finish**		
7a.	Front High Spatial Frequency Roughness (HSFR: $\lambda_{spatial} \leq 1\mu m$)	nm	≤0.15 rms
7b.	Front Mid-Spatial Frequency Roughness (MSFR: $10\mu m \geq \lambda_{spatial} > 1\mu m$)	nm	≤0.2 rms
7c.	Backside Finish		Polished to <5nm rms
8.	**Thermal Properties of the Bulk Material**		
8a.	CTE (20 – 50°C)	ppb/K	0 ±40
8b.	CTE uniformity (within a wafer @20°C)	ppb/K	Mean ± 10 TIR
9.	**Bulk defect density**		**(Under development)**

IV. Notes for each specification.

1. The diameter of the mask substrate is the same as the SEMI standard 200mm silicon wafer (notched) to ensure that it will be properly handled by robotic equipment of the inspection and deposition tools and the ETS. A new 152mm square mask format with a substrate thickness of 6.35mm is being developed.

2. The current thickness specification is the same as that for a standard 200mm silicon wafer. (see note no. 1)

3. GTIR is the smallest distance between two planes, both parallel to the least-squares reference plane, which enclose all points on the front surface of the wafer (except for a 10mm exclusion zone on the edge of the wafer). This is to ensure that any low-spatial frequency height fluctuation is correctable by the ETS.

4. Because the substrate will be electrostatically mounted on the ETS, any nonuniformity in substrate thickness will appear as height fluctuation on the front surface.

5. The condenser optics directs the EUV light into a smile-shaped "ring field" that can be completely enclosed in a rectangle of 16mm x 110mm. During printing, it is scanned across an area outlined by the dashed line and labeled "Area to be printed" in Fig. 1. For simplicity, we defined the *Quality Area* to be a rectangular area of 130mm x 110mm that encompasses the whole area to be printed, and the *Site Area* to be *any* rectangular sub-area of 16mm x 110mm inside the Quality Area that would completely enclose an area under illumination of the ring field. SFSR is the smallest distance between two planes, both parallel to the least-squares reference plane of the Site Area, which encloses all points in the Site Area.

Figure 1: Dimensions of the Quality Area and the Site Area of the EUVL mask. Red (dashed) lines represent the curved areas to be printed and under illumination. For simplicity, we defined the Quality and Site Areas to be rectangular, as shown by the blue (solid) lines.

5. (cont'd) The reason for our tight flatness specification is because imaging is non-telecentric in EUVL (Fig.2) and is very sensitive to image-placement distortion. The height variation of any area under illumination must be ≤0.2μm in order for the image placement distortion to stay within the error budget.

Image placement distortion
$$= \Delta h \tan^\theta /M$$

Figure 2: Non-telecentric illumination causes any non-uniformity in height to produce an image-placement distortion. The reduction factor M is 4 for the Experimental Test Stand.
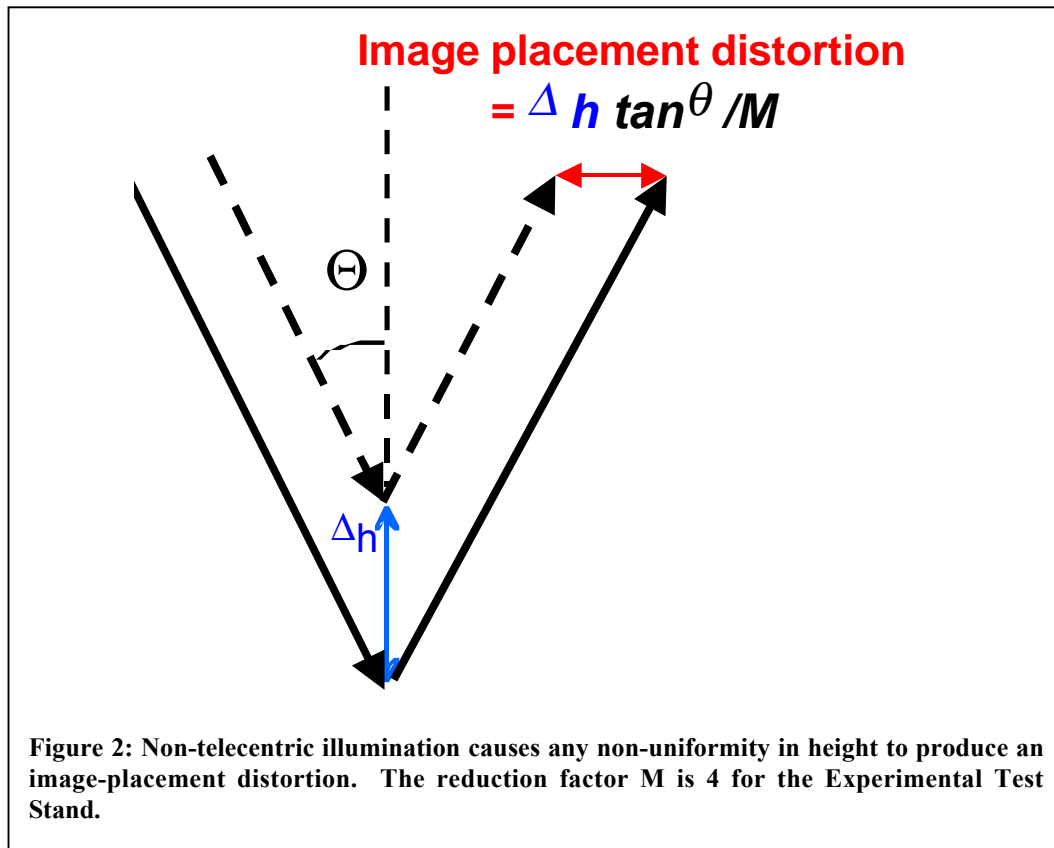
6. The mask lies on the image plane, and any mask surface defect that is on the order of the smallest isolated feature size on the wafer may print. Currently, the smallest light point defect (LPD) we specify is 80nm (the sizes of the defects are subject to be revised in the future). A LPD is any defect detected with laser light scattering inspection. The size is calibrated to the amount of light scattered by a reference polystyrene latex sphere of the indicated diameter resting on the surface being inspected. In general, one needs to be concerned about defects greater than 1/5 the Critical Dimension (CD). For a 100nm CD, the smallest printed defect size of concern is 20nm, which corresponds to a defect on the mask that is 80nm due to the 4x reduction in the ETS projection optics. Defects in the exclusion zone do not count.

7. The roughness specifications are divided into High Spatial Frequency Roughness (HSFR) and Mid-Spatial Frequency Roughness (MSFR). Roughness in the two re-gimes would have different impact on printing: HSFR scatters light out of the entrance pupil and represents a loss of brightness, whereas MSFR leads to small angle scattering and results in image speckle[1]. Backside finish specification is driven both by the need for a reflective back surface for performing interferometry on the substrate and by reducing the potential for a rough back surface to trap particles.

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8a. The absolute value of the CTE between different mask substrates must be within 40 ppb/K to eliminate the need for magnification correction between a wafer change during printing.

8b. The variation of the CTE from site to site within the mask substrate must also be maintained to within 10ppb of the mean CTE value specified in note no. 8a to minimize image placement distortion.

9. Bulk defects do not directly affect EUV lithography. Because the mask is reflective, only surface defects on the mask substrate are important. However, in shaping the mask substrate from bulk substrate material, a larger piece is sliced, lapped, and polished to form the mask substrate. Bulk material defects might manifest themselves as surface defects if they happen to lie on or near the plane that forms the final mask substrate surface. An acceptable bulk defect density is being developed based on the calculated probability that defects might be in or near the substrate surface plane.

V.   Acknowledgment

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[1] T.D. Milster & N.A.Beaudry "Scattering and coherence in EUVL", in *Emerging Lithographic Technologies II*, *Y. Vladimirsky, ed., Proc. SPIE*, **3331**, pp.537-43, (1998).